FERNANDO GARCÍA REDONDO

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SUMMARY

- Over 15 years of hands on experience on electronic systems research.
- Emerging memory devices modeling and simulation, from physical compact model to system.
- HW aware algorithm optimization –TinyML, Compute-in-memory and Probabilistic Computing architectures and algorithms design for constrained devices.

PROFESSIONAL EXPERIENCE

IMEC

2022 - Present PRINCIPAL MEMBER OF TECHNICAL STAFF AND TEAM LEADER

- Technology & Circuit Enablement Team Leader. Technical manager and supervisor of >10 people.
- Magnetics Program Leadership.
- Regular interface to system/memory partners.
- Emerging memories modeling and circuit design: from device to macro to test-chips.
  - Design/System Technology Co-optimization (DTCO/STCO).
  - Emerging memories: MRAM, SRAM, IGZO-based eDRAM, 3D-DRAM, 3D-IGZO CCD.
  - Testchips architecture, digital design, Analog-Mix-Signal flows and testing infrastructure.
- Probabilistic compute and Compute-in-Memory systems HW/SW co-design.
- IP Generation and dissemination.

ARM RESEARCH, ARM LTD.

2018 - 2022 STAFF RESEARCH ENGINEER

- HW aware algorithm optimization. Design of ultra low power always-ON MCU running realtime KWS –10μW active 10nW sleep Cortex M33 with 16KB of RAM and 128KB of ROM.
- Analog ML Compute-in-Memory systems HW/SW co-design.
- Stochastic analysis and numerical modeling of NVM memories. MRAM Compact model for efficient simulation and circuitry design for reliable operation.
- Design of AMS platform for the modeling and simulation of Intermittent Compute (IC) Systems.
- Design of Energy-Harvesting power control and testbed platform –including Gen2 RFID reader SDK development, RF agents, PCB and lab-equipment orchestration.
- IP Generation and dissemination.

UNIVERSIDAD P. C. ICAI

2017 ASSOCIATE LECTURER

Associate Lecturer in Integrated Circuit Design. Course coordinator.

UNIVERSIDAD POLITÉCNICA DE MADRID

2017 POSTDOCTORAL RESEARCHER

Design and simulation of RRAM-CMOS based circuit applications

2012-2017 PH.D. CANDIDATE *Resistive RAM: Simulation and Modeling for Reliable Design*

2010-2013 RESEARCH GRANT

RTL design and implementation of radar and communication systems.

NEXUS 5

2006 - 2009 SOFTWARE ENGINEER

HONORS & AWARDS

2019 Extraordinary Doctorate Awards, Universidad Politécnica de Madrid.

2012 Degree with Honors, Final Degree Project, BSc.

EDUCATION

UNIVERSIDAD POLITÉCNICA DE MADRID

2017 PH.D. IN ELECTRONIC SYSTEMS ENGINEERING

2012 MSC. IN ELECTRONIC SYSTEMS ENGINEERING

2011 BSC + MSC (ABET ACCREDITED) IN TELECOMMUNICATION ENGINEERING

SELECTED RESEARCH DISSEMINATION AND IP GENERATION

2026 *Backside Split-VDD Write-Assist Driven SRAM Macro Scaling in Nanosheet-Era.* IEEE VLSI.

2025 *IGZO based eDRAM: Bitcell and Array Optimization Enabling Denser LLC.* IEEE ESSERC.

2022 *Ml-hw co-design of noise-robust tinyml models and always-on analog CIM edge acc..* IEEE Micro.

2020 *27.2 MoNo: A performance-regulated 0.8-to-38MHz DVFS ARM cortex-M33 SIMD MCU with 10nW sleep power.* IEEE ISSCC.

2019 *Applications of computation-in-memory architectures based on memristive devices.* IEEE DATE.

2016 *SPICE CM. of bipolar/unipolar memristor switching governed by electrical thresholds.* IEEE TCAS-I.

PATENTS

Arm/Imec have filed >30 patent applications on which I am a named inventor, addressing memory bitcell and circuitry, CiM ML accelerators, low power systems, IC systems and NVM memories.